

7. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?
- (a) $A_3A_2A_1A_0 = 1010$ (b) $A_3A_2A_1A_0 = 1110$
 (c) $A_3A_2A_1A_0 = 1100$ (d) $A_3A_2A_1A_0 = 0100$
8. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are
- (a) a, c, f, g (b) b, c, f, g
 (c) b, c, e, f (d) b, d, e, g
9. If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active-HIGH binary output is
- (a) 110 (b) 010
 (c) 101 (d) 000
10. In general, a multiplexer has
- (a) one data input, several data outputs, and selection inputs
 (b) one data input, one data output, and one selection input
 (c) several data inputs, several data outputs, and selection inputs
 (d) several data inputs, one data output, and selection inputs
11. Data distributors are basically the same as
- (a) decoders (b) demultiplexers
 (c) multiplexers (d) encoders
12. Which of the following codes exhibit even parity?
- (a) 10011000 (b) 01111000
 (c) 11111111 (d) 11010101
 (e) all (f) both answers (b) and (c)

PROBLEMS

Answers to odd-numbered problems are at the end of the book.

Section 6-1 Half and Full Adders

1. For the full-adder of Figure 6-4, determine the outputs for each of the following inputs
- (a) $A = 0, B = 1, C_{in} = 0$ (b) $A = 1, B = 0, C_{in} = 1$
 (c) $A = 0, B = 0, C_{in} = 0$
2. What are the half-adder inputs that will produce the following outputs:
- (a) $\Sigma = 0, C_{out} = 0$ (b) $\Sigma = 1, C_{out} = 0$
 (c) $\Sigma = 0, C_{out} = 1$
3. Determine the outputs of a full-adder for each of the following inputs:
- (a) $A = 1, B = 0, C_{in} = 0$ (b) $A = 0, B = 0, C_{in} = 1$
 (c) $A = 0, B = 1, C_{in} = 1$ (d) $A = 1, B = 1, C_{in} = 1$

Section 6-2 Parallel Binary Adders

4. For the parallel adder in Figure 6-69, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.

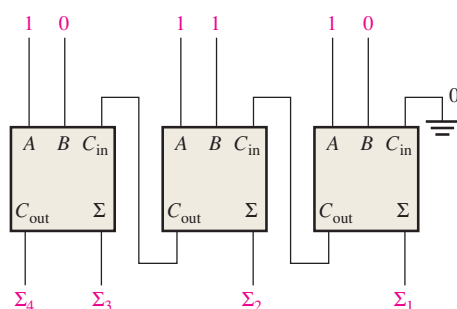


FIGURE 6-69

5. Repeat Problem 4 for the circuit and input conditions in Figure 6–70.

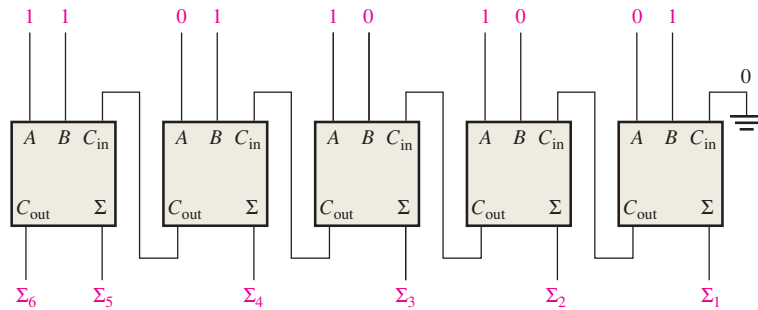


FIGURE 6-70

6. The circuit shown in Figure 6–71 is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a) Explain what happens when the $\overline{Add/Subt.}$ input is HIGH. (b) What happens when $\overline{Add/Subt.}$ is LOW?

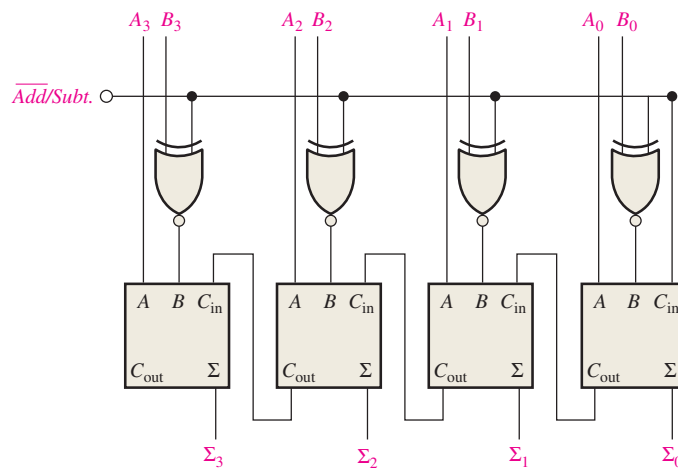


FIGURE 6-71

7. For the circuit in Figure 6–71, assume the inputs are $\overline{Add/Subt.} = 1$, $A = 1010$, and $B = 1101$. What is the output?

8. The input waveforms in Figure 6–72 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

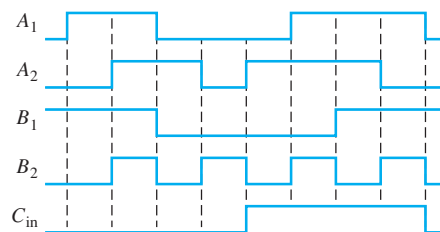


FIGURE 6-72

9. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

10. In the process of checking a 74HC283 4-bit parallel adder, the following logic levels are observed on its pins: 1-HIGH, 2-HIGH, 3-HIGH, 4-HIGH, 5-LOW, 6-LOW, 7-LOW, 9-HIGH, 10-LOW, 11-HIGH, 12-LOW, 13-HIGH, 14-HIGH, and 15-HIGH. Determine if the IC is functioning properly.

Section 6-3 Ripple Carry and Look-Ahead Carry Adders

11. Each of the eight full-adders in an 8-bit parallel ripple carry adder exhibits the following propagation delay:

A to Σ and C_{out} :	20 ns
B to Σ and C_{out} :	20 ns
C_{in} to Σ :	30 ns
C_{in} to C_{out} :	25 ns

Determine the maximum total time for the addition of two 8-bit numbers.

12. Show the additional logic circuitry necessary to make the 4-bit look-ahead carry adder in Figure 6-17 into a 5-bit adder.

Section 6-4 Comparators

13. The waveforms in Figure 6-73 are applied to the comparator as shown. Determine the output ($A = B$) waveform.

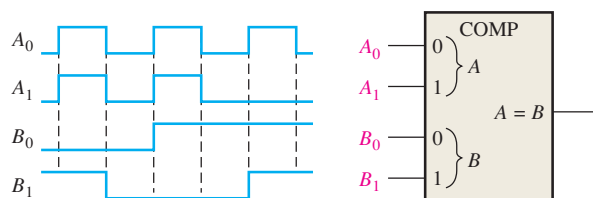


FIGURE 6-73

14. For the 4-bit comparator in Figure 6-74, plot each output waveform for the inputs shown. The outputs are active-HIGH.

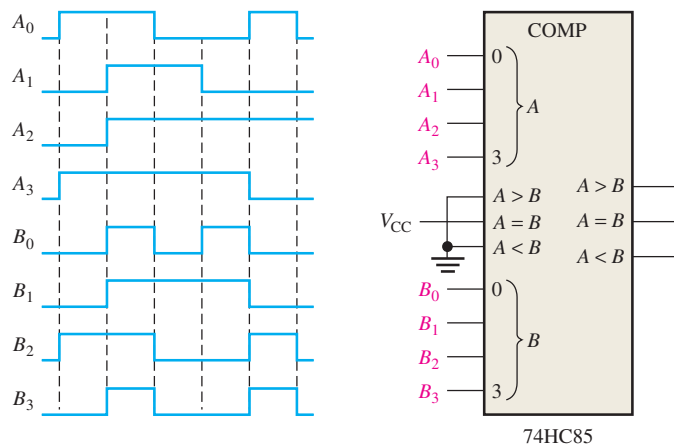


FIGURE 6-74

15. For each set of binary numbers, determine the output states for the comparator of Figure 6–21.

- (a) $A_3A_2A_1A_0 = 1010$ (b) $A_3A_2A_1A_0 = 1101$ (c) $A_3A_2A_1A_0 = 1001$
 $B_3B_2B_1B_0 = 1101$ $B_3B_2B_1B_0 = 1101$ $B_3B_2B_1B_0 = 1000$

Section 6–5 Decoders

16. When a LOW is on the output of each of the decoding gates in Figure 6–75, what is the binary code appearing on the inputs? The MSB is A_3 .

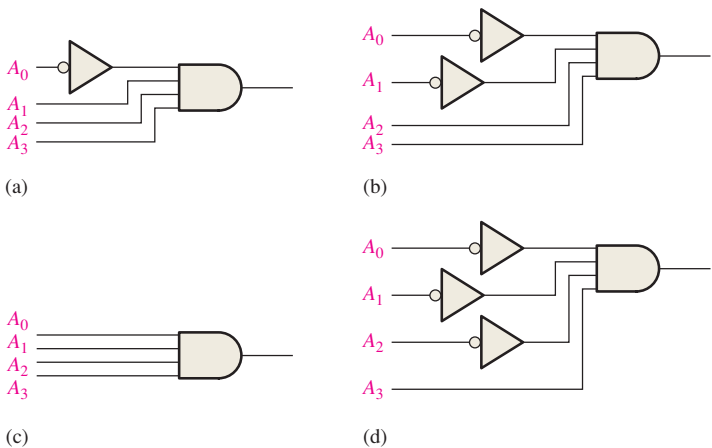


FIGURE 6–75

17. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required:

- (a) 1101 (b) 1000 (c) 11011 (d) 11100
 (e) 101010 (f) 111110 (g) 000101 (h) 1110110

18. Solve Problem 17, given that an active-LOW (0) output is required.

19. You wish to detect only the presence of the codes 1010, 1100, 0001, and 1011. An active-HIGH output is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be LOW.

20. If the input waveforms are applied to the decoding logic as indicated in Figure 6–76, sketch the output waveform in proper relation to the inputs.

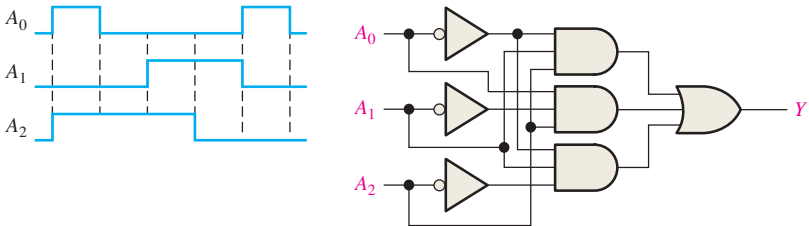


FIGURE 6–76

21. BCD numbers are applied sequentially to the BCD-to-decimal decoder in Figure 6-77. Draw a timing diagram, showing each output in the proper relationship with the others and with the inputs.

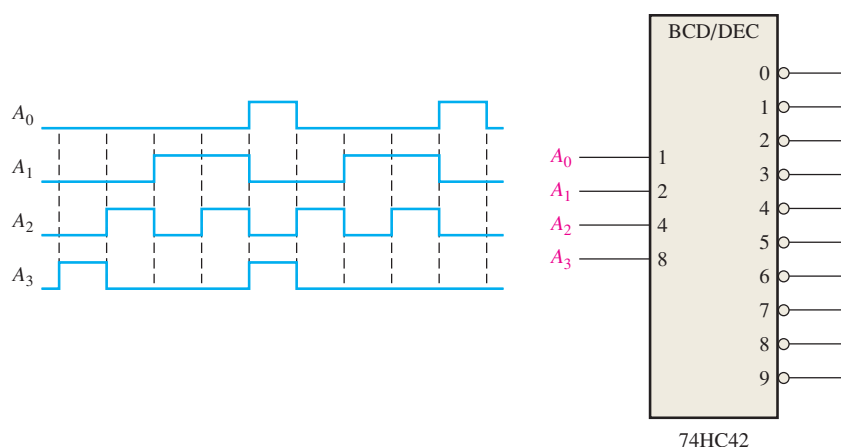


FIGURE 6-77

22. A 7-segment decoder/driver drives the display in Figure 6-78. If the waveforms are applied as indicated, determine the sequence of digits that appears on the display.

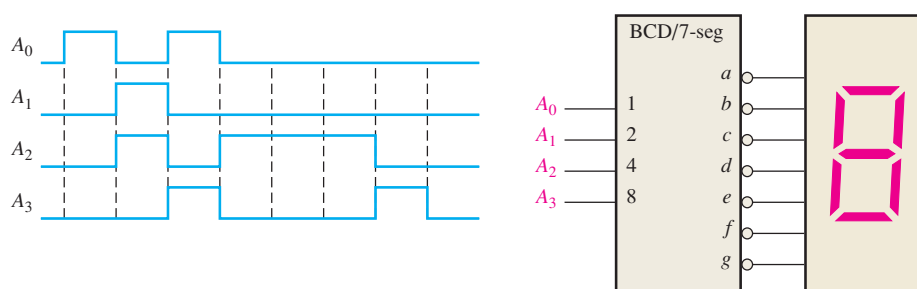


FIGURE 6-78

Section 6-6 Encoders

23. For the decimal-to-BCD encoder logic of Figure 6-37, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD (8421) code?
24. A 74HC147 encoder has LOW levels on pins 2, 5, and 12. What BCD code appears on the outputs if all the other inputs are HIGH?

Section 6-7 Code Converters

25. Convert each of the following decimal numbers to BCD and then to binary.
- (a) 4 (b) 7 (c) 12 (d) 23 (e) 34
26. Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:
- (a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001
27. Show the logic required to convert a 10-bit Gray code to binary and use that logic to convert the following Gray code words to binary:
- (a) 1010111100 (b) 1111000011 (c) 1011110011 (d) 1000000001

Section 6-8 Multiplexers (Data Selectors)

28. For the multiplexer in Figure 6-79, determine the output for the following input states: $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 1$, $S_0 = 0$, $S_1 = 1$.

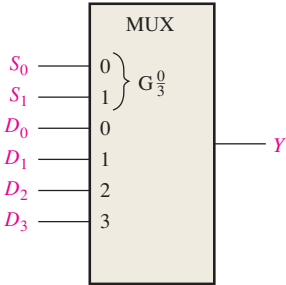


FIGURE 6-79

29. If the data-select inputs to the multiplexer in Figure 6-79 are sequenced as shown by the waveforms in Figure 6-80, determine the output waveform with the data inputs specified in Problem 28.

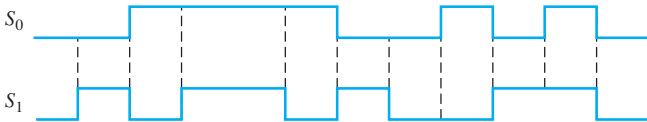


FIGURE 6-80

30. The waveforms in Figure 6-81 are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the Y output waveform.

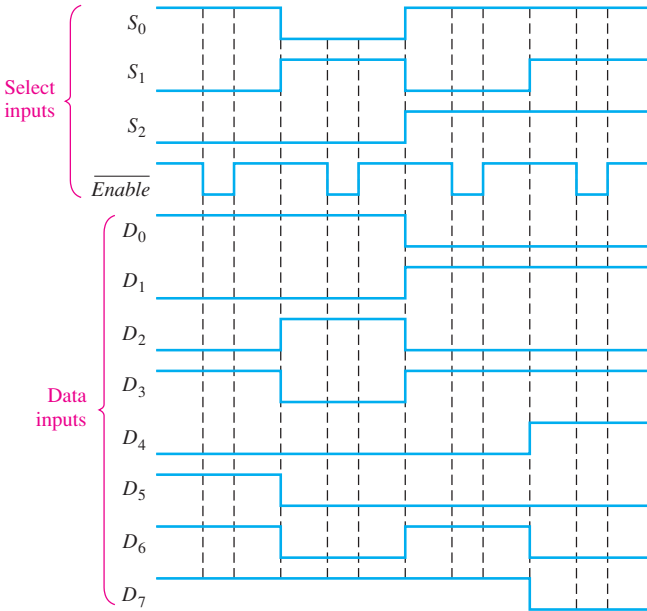


FIGURE 6-81

Section 6-9 Demultiplexers

31. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.

Section 6-10 Parity Generators/Checkers

32. The waveforms in Figure 6-82 are applied to the 4-bit parity logic. Determine the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.

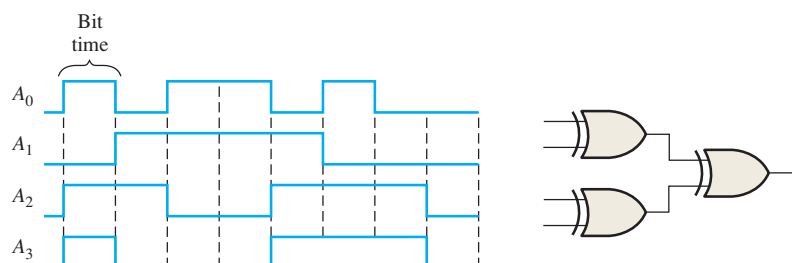


FIGURE 6-82

33. Determine the Σ Even and the Σ Odd outputs of a 74HC280 9-bit parity generator/checker for the inputs in Figure 6-83. Refer to the function table in Figure 6-56.

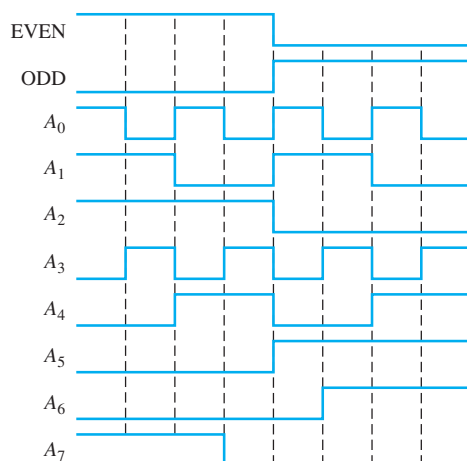


FIGURE 6-83

Section 6-11 Troubleshooting

34. The full-adder in Figure 6-84 is tested under all input conditions with the input waveforms shown. From your observation of the Σ and C_{out} waveforms, is it operating properly, and if not, what is the most likely fault?

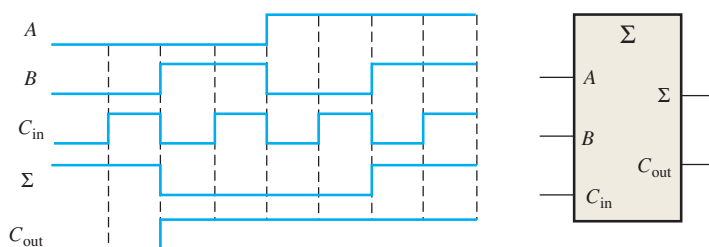


FIGURE 6-84

35. List the possible faults for each decoder/display in Figure 6–85.

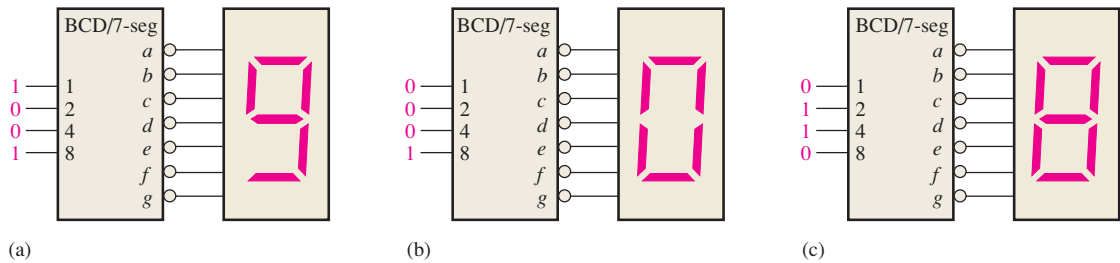


FIGURE 6-85

36. Develop a systematic test procedure to check out the complete operation of the keyboard encoder in Figure 6–39.
37. You are testing a BCD-to-binary converter consisting of 4-bit adders as shown in Figure 6–86. First verify that the circuit converts BCD to binary. The test procedure calls for applying BCD numbers in sequential order beginning with 0_{10} and checking for the correct binary output. What symptom or symptoms will appear on the binary outputs in the event of each of the following faults? For what BCD number is each fault *first* detected?
- (a) The A_1 input is open (top adder).
 - (b) The C_{out} is open (top adder).
 - (c) The Σ_4 output is shorted to ground (top adder).
 - (d) The 32 output is shorted to ground (bottom adder).

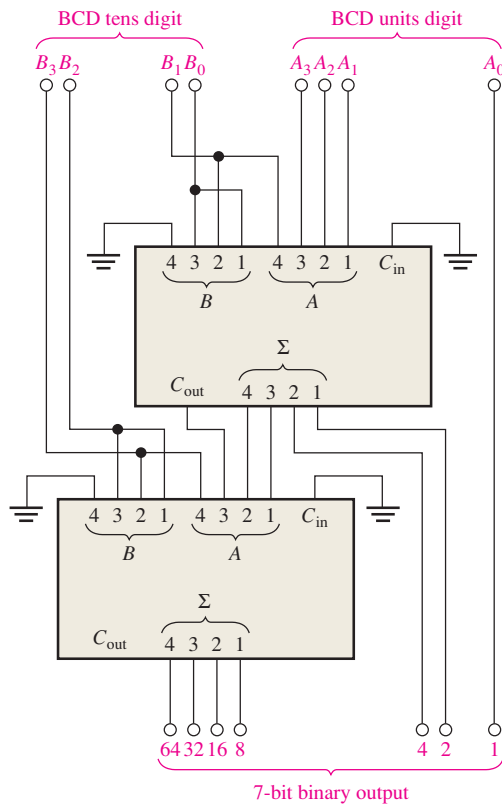


FIGURE 6-86

38. For the 7-segment display multiplexing system in Figure 6–49, determine the most likely cause or causes for each of the following symptoms:
- The *B*-digit (MSD) display does not turn on at all.
 - Neither 7-segment display turns on.
 - The *f*-segment of both displays appears to be on all the time.
 - There is a visible flicker on the displays.
39. Develop a systematic procedure to fully test the 74HC151 data selector IC.
40. During the testing of the data transmission system in Figure 6–58, a code is applied to the D_0 through D_6 inputs that contains an odd number of 1s. A single bit error is deliberately introduced on the serial data transmission line between the MUX and the DEMUX, but the system does not indicate an error (error output = 0). After some investigation, you check the inputs to the even parity checker and find that D_0 through D_6 contain an even number of 1s, as you would expect. Also, you find that the D_7 parity bit is a 1. What are the possible reasons for the system not indicating the error?
41. In general, describe how you would fully test the data transmission system in Figure 6–58, and specify a method for the introduction of parity errors.

Applied Logic

42. Use a 74HC00 (quad NAND gates) and any other devices that may be required to produce active-HIGH outputs for the given inputs of the state decoder.
43. Implement the light output logic with the 74HC00 if active-LOW outputs are required.

Special Design Problems

44. Modify the design of the 7-segment display multiplexing system in Figure 6–49 to accommodate two additional digits.
45. Using Table 6–2, write the SOP expressions for the Σ and C_{out} of a full-adder. Use a Karnaugh map to minimize the expressions and then implement them with inverters and AND-OR logic. Show how you can replace the AND-OR logic with 74HC151 data selectors.
46. Implement the logic function specified in Table 6–14 by using a 74HC151 data selector.

TABLE 6–14

Inputs				Output
A_3	A_2	A_1	A_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

47. Using two of the 6-position adder modules from Figure 6–13, design a 12-position voting system.
48. The adder block in the tablet-bottling system in Figure 6–87 performs the addition of the 8-bit binary number from the counter and the 16-bit binary number from Register B. The result from

Functions of Combinational Logic

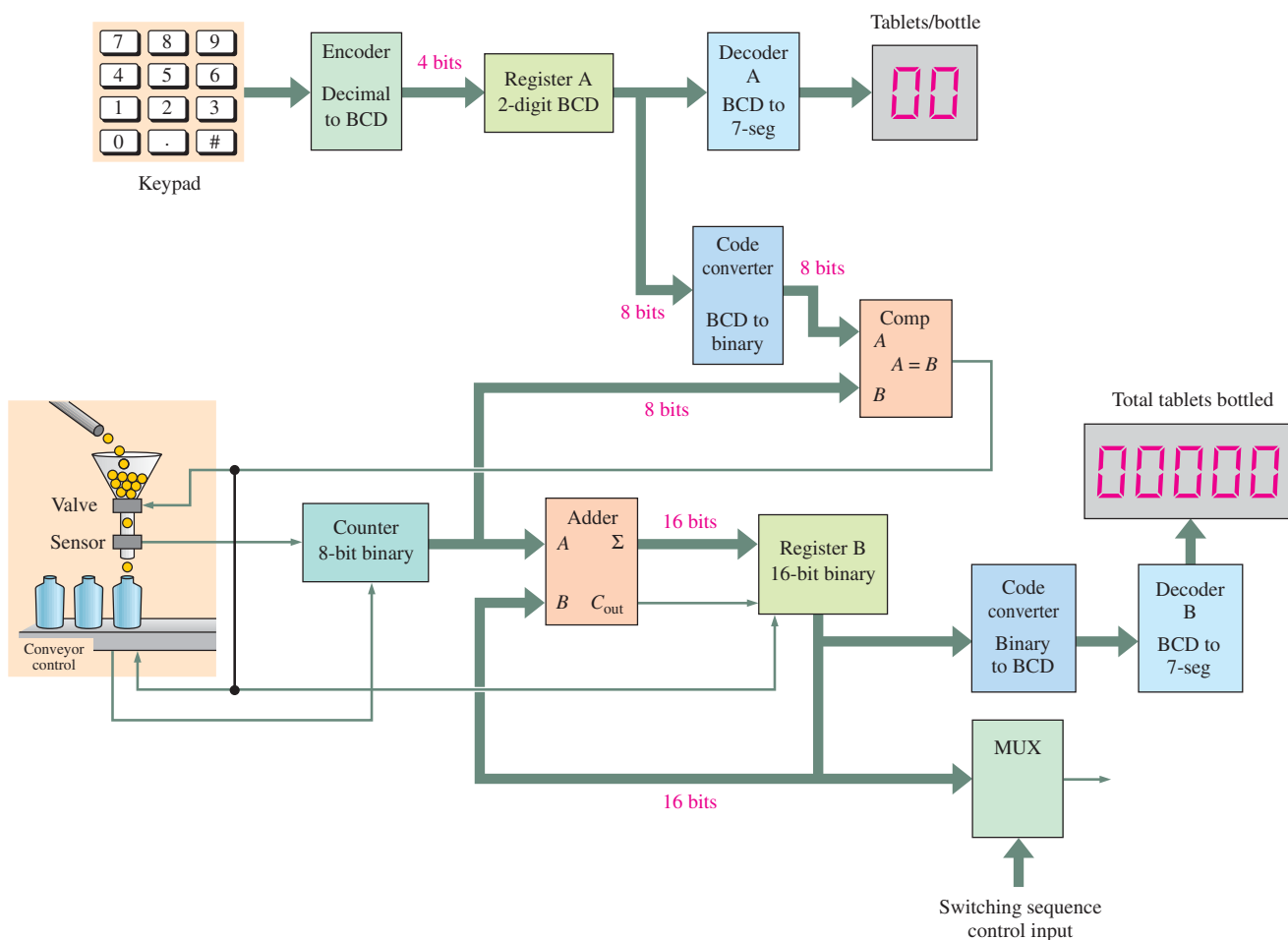


FIGURE 6-87

the adder goes back into Register B. Use 74HC283s to implement this function and draw a complete logic diagram including pin numbers. This is similar to the system in Section 1-4.

49. Use 74HC85s to implement the comparator block in the tablet-bottling system in Figure 6-87 and draw a complete logic diagram including pin numbers. The comparator compares the 8-bit binary number (actually only seven bits are required) from the BCD-to-binary converter with the 8-bit binary number from the counter.
50. Two BCD-to-7-segment decoders are used in the tablet-bottling system in Figure 6-87. One is required to drive the 2-digit *tablets/bottle* display and the other to drive the 5-digit *total tablets bottled* display. Use 74HC47s to implement each decoder and draw a complete logic diagram including pin numbers.
51. The encoder shown in the system block diagram of Figure 6-87 encodes each decimal key closure and converts it to BCD. Use a 74HC147 to implement this function and draw a complete logic diagram including pin numbers.
52. The system in Figure 6-87 requires two code converters. The BCD-to-binary converter changes the 2-digit BCD number in Register A to an 8-bit binary code (actually only 7 bits are required because the MSB is always 0). Use appropriate fixed-function IC code converters to implement the BCD-to-binary converter function and draw a complete logic diagram including pin numbers.

Multisim

Multisim Troubleshooting Practice

53. Open file P06-53. For the specified fault, predict the effect on the circuit. Then introduce the fault and verify whether your prediction is correct.

54. Open file P06-54. For the specified fault, predict the effect on the circuit. Then introduce the fault and verify whether your prediction is correct.
55. Open file P06-55. For the observed behavior indicated, predict the fault in the circuit. Then introduce the suspected fault and verify whether your prediction is correct.
56. Open file P06-56. For the observed behavior indicated, predict the fault in the circuit. Then introduce the suspected fault and verify whether your prediction is correct.

ANSWERS

SECTION CHECKUPS

Section 6-1 Half and Full Adders

1. (a) $\Sigma = 1, C_{\text{out}} = 0$
 (b) $\Sigma = 0, C_{\text{out}} = 0$
 (c) $\Sigma = 1, C_{\text{out}} = 0$
 (d) $\Sigma = 0, C_{\text{out}} = 1$
2. $\Sigma = 1, C_{\text{out}} = 1$

Section 6-2 Parallel Binary Adders

1. $C_{\text{out}} \Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 11001$
2. Three 74HC283s are required to add two 10-bit numbers.

Section 6-3 Ripple Carry and Look-Ahead Carry Adders

1. $C_g = 0, C_p = 1$
2. $C_{\text{out}} = 1$

Section 6-4 Comparators

1. $A > B = 1, A < B = 0, A = B = 0$ when $A = 1011$ and $B = 1010$
2. Right comparator: $A < B = 1; A = B = 0; A > B = 0$
 Left comparator: $A < B = 0; A = B = 0; A > B = 1$

Section 6-5 Decoders

1. Output 5 is active when 101 is on the inputs.
2. Four 74HC154s are used to decode a 6-bit binary number.
3. Active-HIGH output drives a common-cathode LED display.

Section 6-6 Encoders

1. (a) $A_0 = 1, A_1 = 1, A_2 = 0, A_3 = 1$
 (b) No, this is not a valid BCD code.
 (c) Only one input can be active for a valid output.
2. (a) $\bar{A}_3 = 0, \bar{A}_2 = 1, \bar{A}_1 = 1, \bar{A}_0 = 1$
 (b) The output is 0111, which is the complement of 1000 (8).

Section 6-7 Code Converters

1. $10000101 (\text{BCD}) = 1010101_2$
2. An 8-bit binary-to-Gray converter consists of seven exclusive-OR gates in an arrangement like that in Figure 6-40 but with inputs B_0 – B_7 .

Section 6-8 Multiplexers (Data Selectors)

1. The output is 0.
2. (a) 74HC153: Dual 4-input data selector/multiplexer
 (b) 74HC151: 8-input data selector/multiplexer

3. The data output alternates between LOW and HIGH as the data-select inputs sequence through the binary states.
4. (a) The 74HC157 multiplexes the two BCD codes to the 7-segment decoder.
(b) The 74HC47 decodes the BCD to energize the display.
(c) The 74HC139 enables the 7-segment displays alternately.

Section 6-9 Demultiplexers

1. A decoder can be used as a multiplexer by using the input lines for data selection and an Enable line for data input.
2. The outputs are all HIGH except D_{10} , which is LOW.

Section 6-10 Parity Generators/Checkers

1. (a) Even parity: $\underline{1}110100$ (b) Even parity: $\underline{0}01100011$
2. (a) Odd parity: $\underline{1}1010101$ (b) Odd parity: $\underline{1}1000001$
3. (a) Code is correct, four 1s. (b) Code is in error, seven 1s

Section 6-11 Troubleshooting

1. A glitch is a very short-duration voltage spike (usually unwanted).
2. Glitches are caused by transition states.
3. Strobe is the enabling of a device for a specified period of time when the device is not in transition.

RELATED PROBLEMS FOR EXAMPLES

6-1 $\Sigma = 1, C_{\text{out}} = 1$

6-2 $\Sigma_1 = 0, \Sigma_2 = 0, \Sigma_3 = 1, \Sigma_4 = 1$

6-3 $1011 + 1010 = 10101$

6-4 See Figure 6-88.

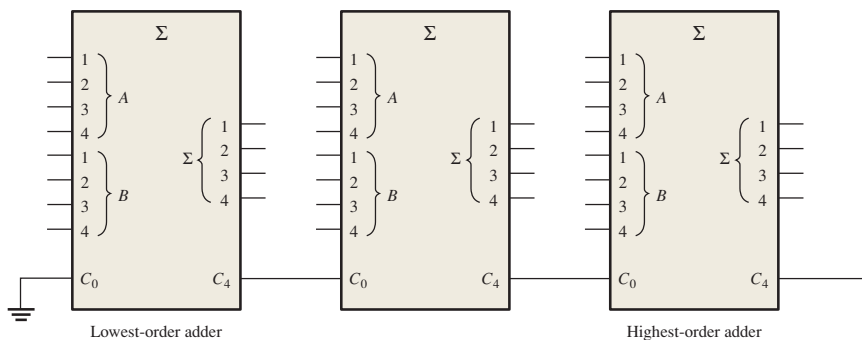


FIGURE 6-88

6-5 See Figure 6-89.

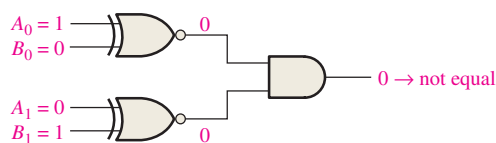


FIGURE 6-89

6-6 $A > B = 0, A = B = 0, A < B = 1$

6-7 See Figure 6-90.

6-8 See Figure 6-91.

6-9 Output 22

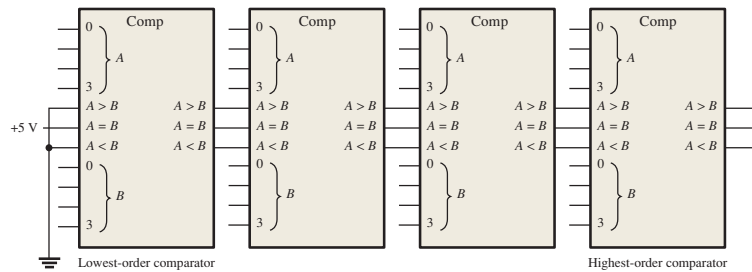


FIGURE 6-90

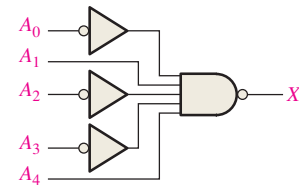


FIGURE 6-91

6-10 See Figure 6-92.

6-11 All inputs LOW: $\bar{A}_0 = 0, \bar{A}_1 = 1, \bar{A}_2 = 1, \bar{A}_3 = 0$

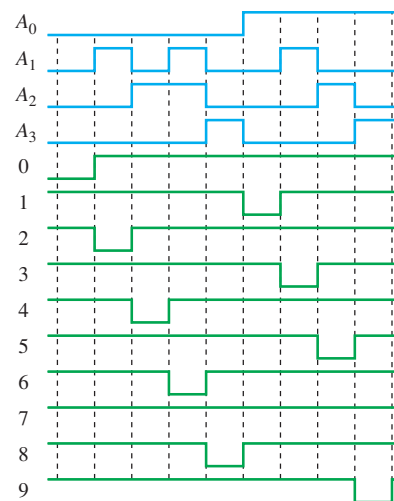


FIGURE 6-92

All inputs HIGH: All outputs HIGH.

6-12 BCD 01000001

	00000001	1
	00101000	40
Binary	00101001	41

6-13 Seven exclusive-OR gates

6-14 See Figure 6-93.

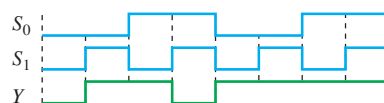


FIGURE 6-93

- 6-15 $D_0: S_3 = 0, S_2 = 0, S_1 = 0, S_0 = 0$
 $D_4: S_3 = 0, S_2 = 1, S_1 = 0, S_0 = 0$
 $D_8: S_3 = 1, S_2 = 0, S_1 = 0, S_0 = 0$
 $D_{13}: S_3 = 1, S_2 = 1, S_1 = 0, S_0 = 1$

6-16 See Figure 6-94.

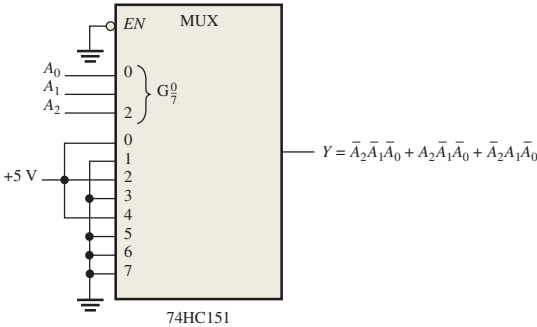


FIGURE 6-94

6-17 See Figure 6-95.

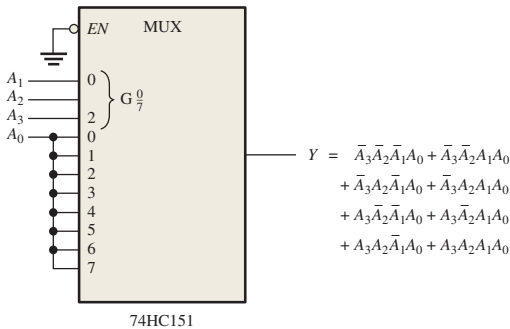


FIGURE 6-95

6-18 See Figure 6-96.

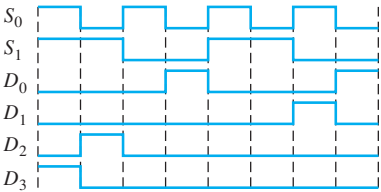


FIGURE 6-96

TRUE/FALSE QUIZ

1. T 2. F 3. F 4. F 5. T
6. F 7. T 8. F 9. T 10. F

SELF-TEST

1. (a) 2. (b) 3. (a) 4. (b) 5. (d) 6. (c)
7. (c) 8. (b) 9. (a) 10. (d) 11. (b) 12. (f)